Figure 1a

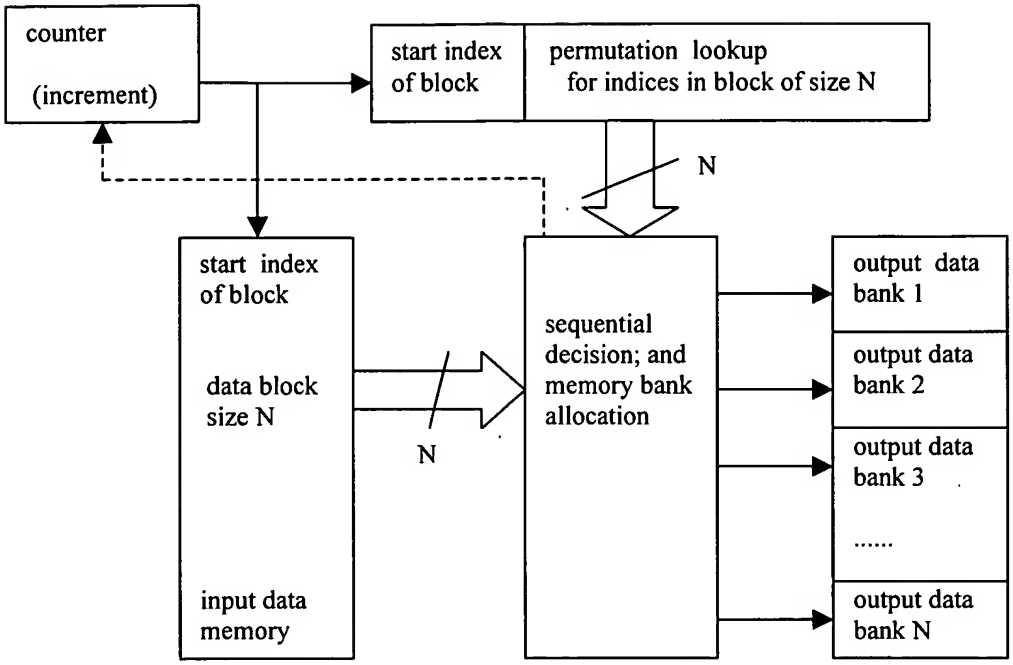
counter
(increment)
start index of block
permutation lookup for indices in block of size N
N
start index of block
data block size N
input data memory
N
sequential decision; and memory bank allocation
output data bank 1
output data bank 2
output data bank 3
.....
output data bank N

Figure 1b

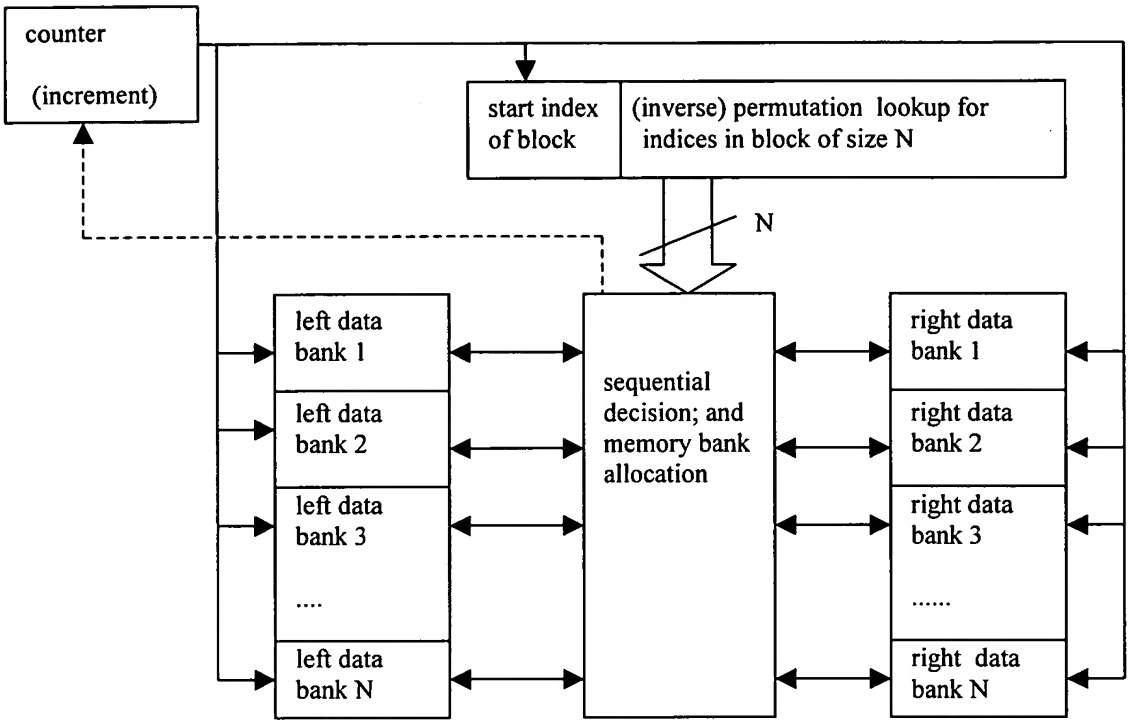
counter
(increment)
start index of block
(inverse) permutation lookup for indices in block of size N
N
left data bank 1
left data bank 2
left data bank 3
....
left data bank N
sequential decision; and memory bank allocation
right data bank 1
right data bank 2
right data bank 3
.....
right data bank N

Figure 2a (prior art)

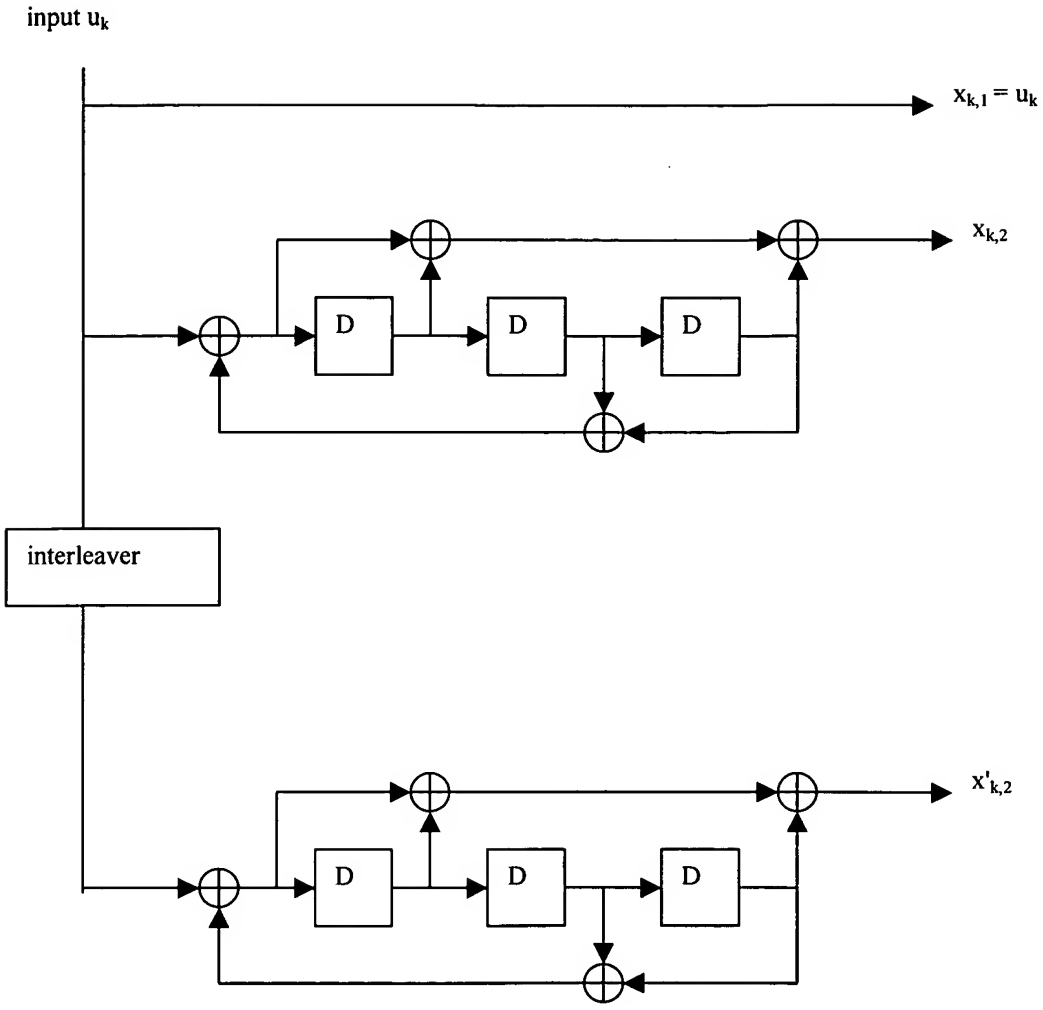

Figure 2b (prior art)

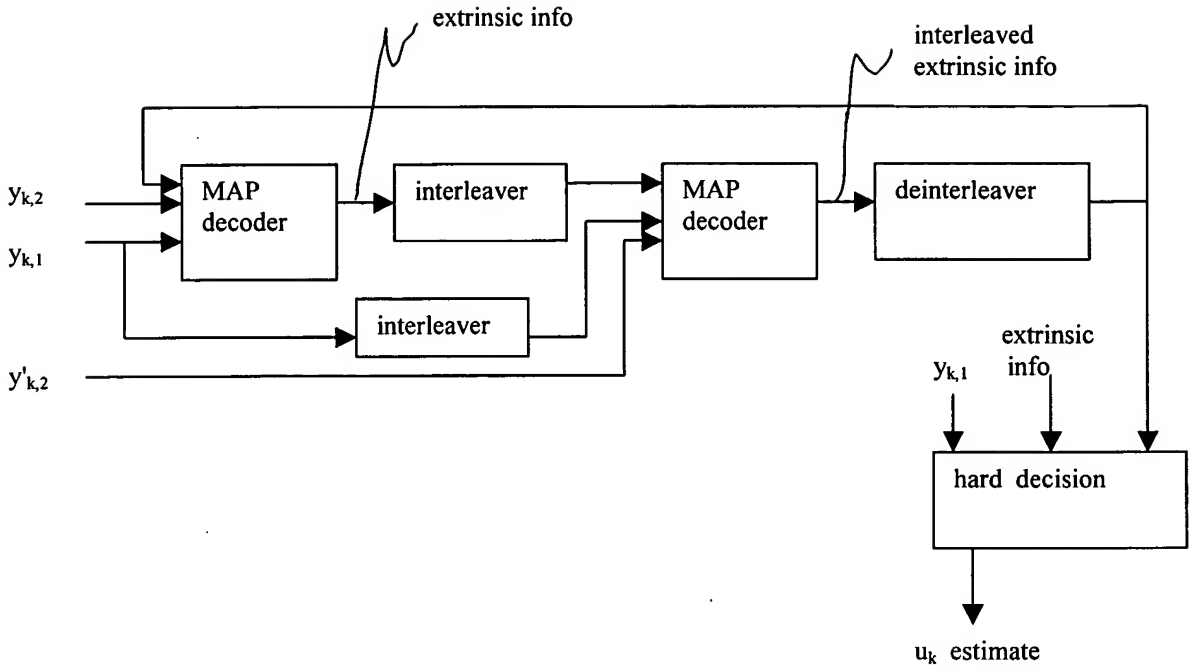

Figure 2c (prior art)

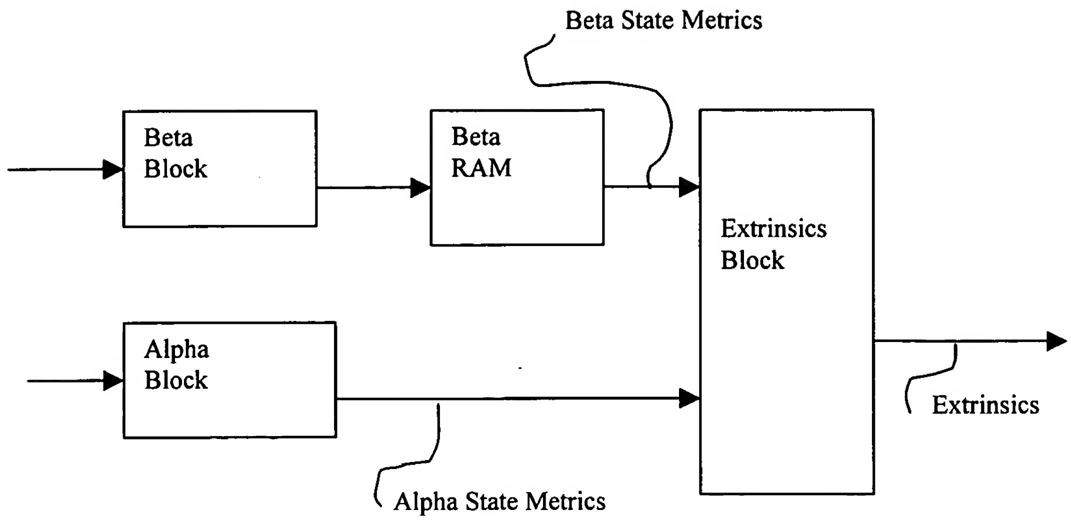

Figure 2d beta block (prior art)

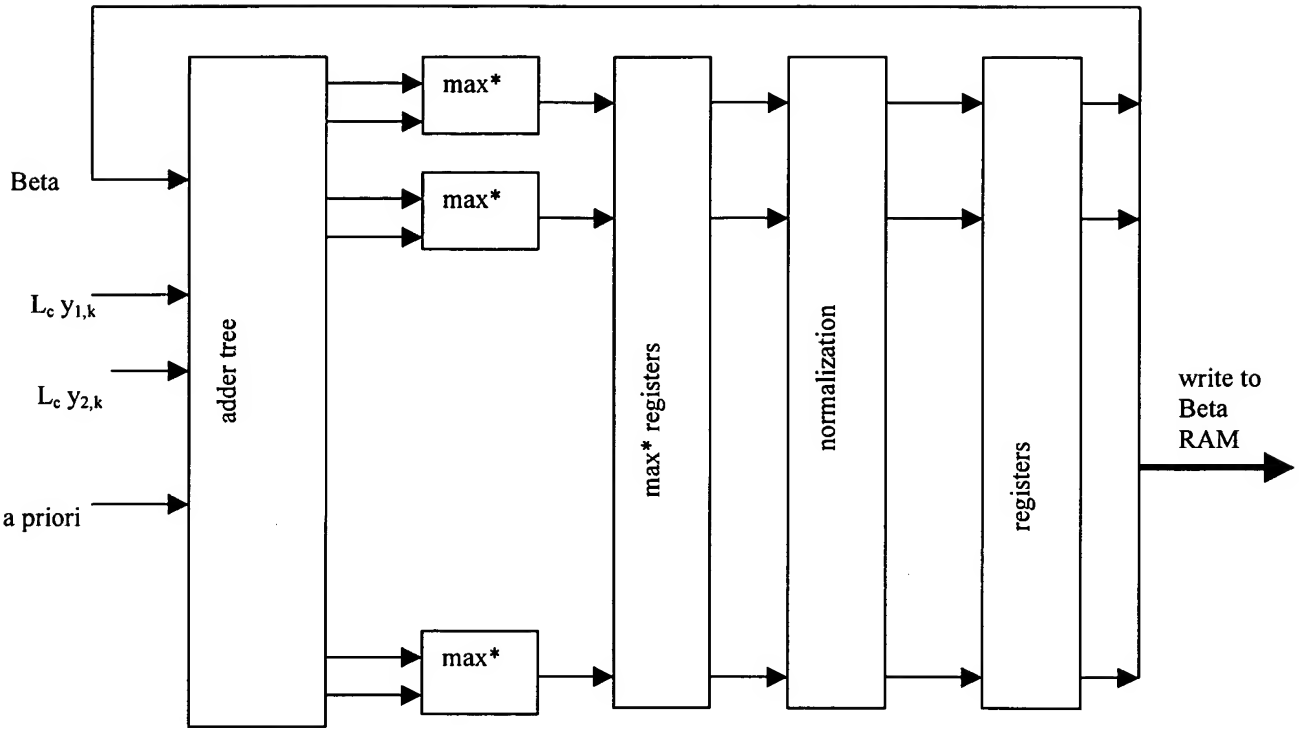

Figure 2e alpha block

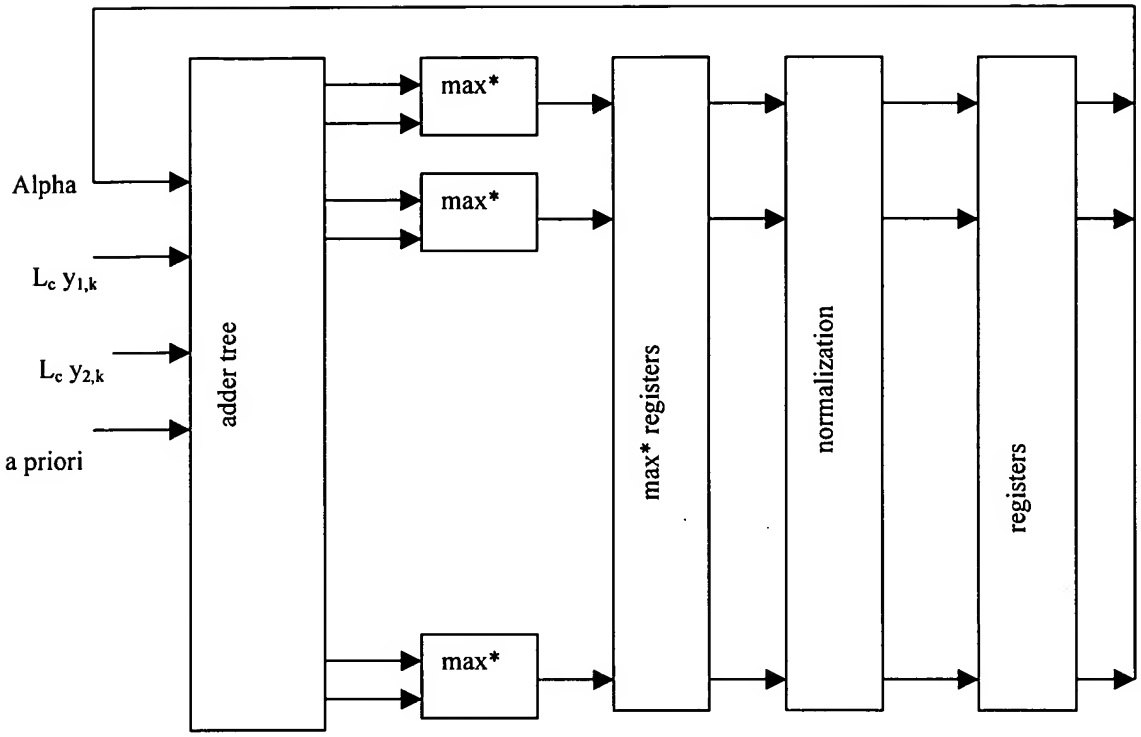

Figure 2f extrinsic block (prior art)

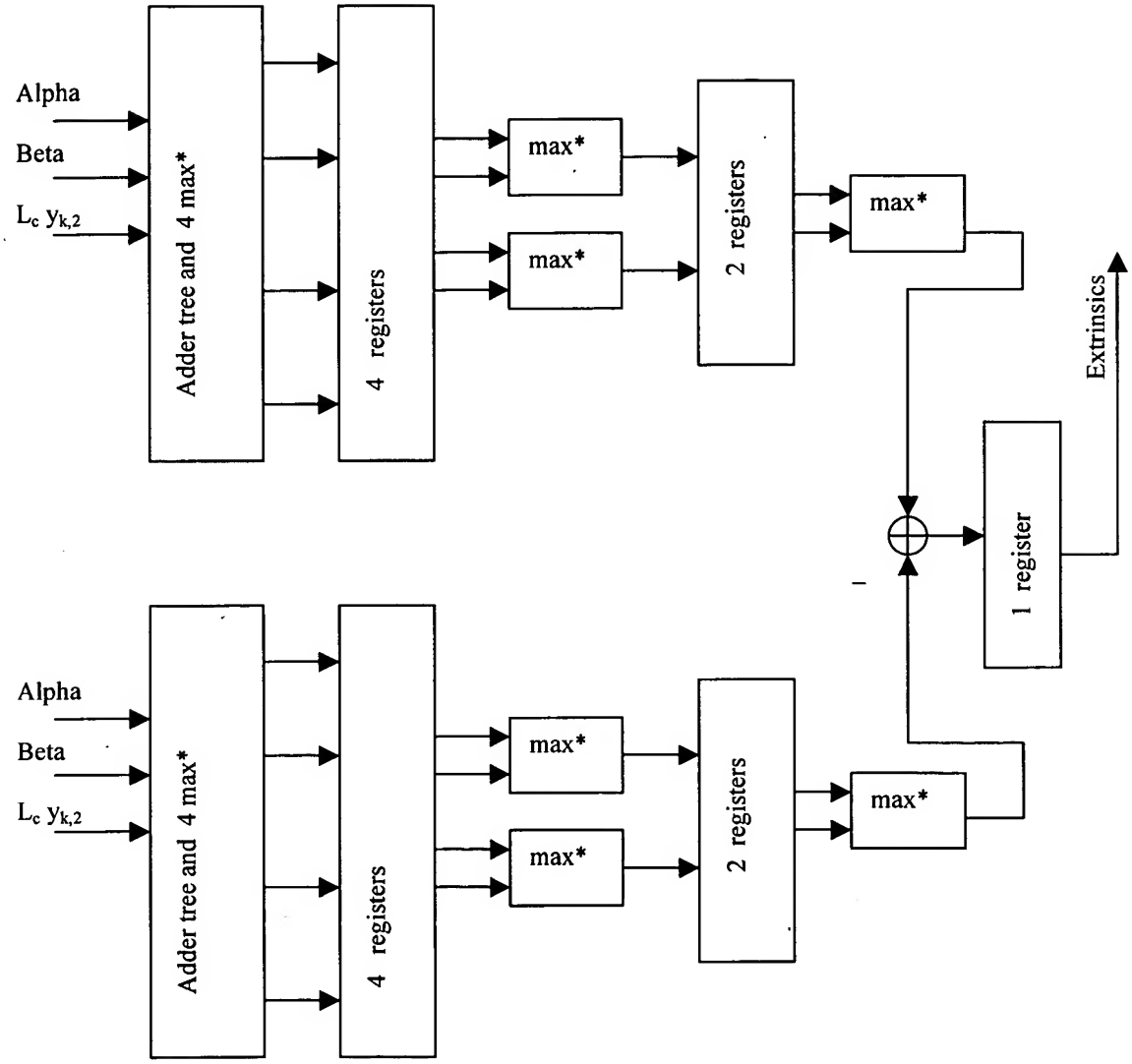

Figure 2g adder plus max* circuit (prior art)

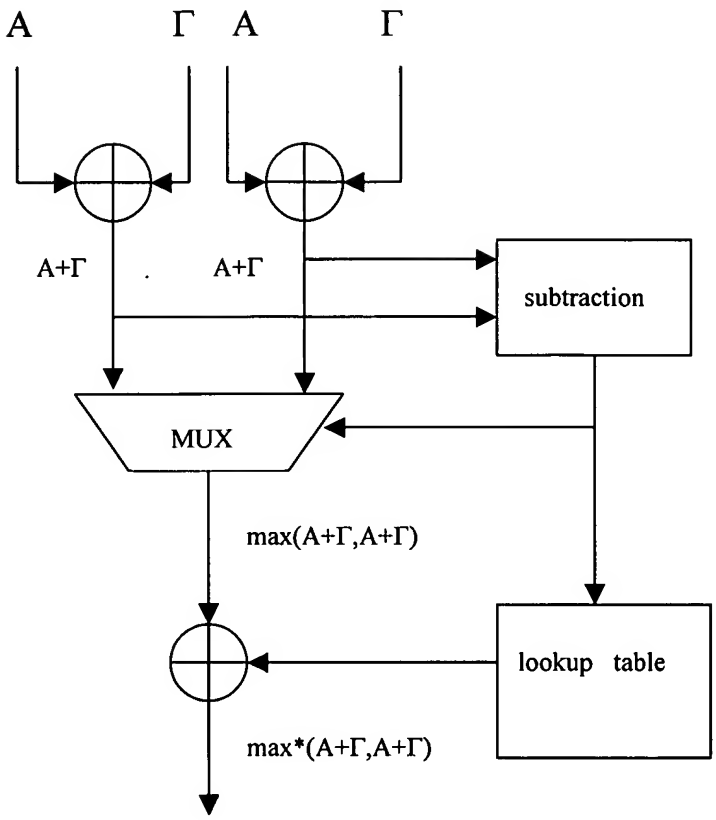

Figure 3a alpha block

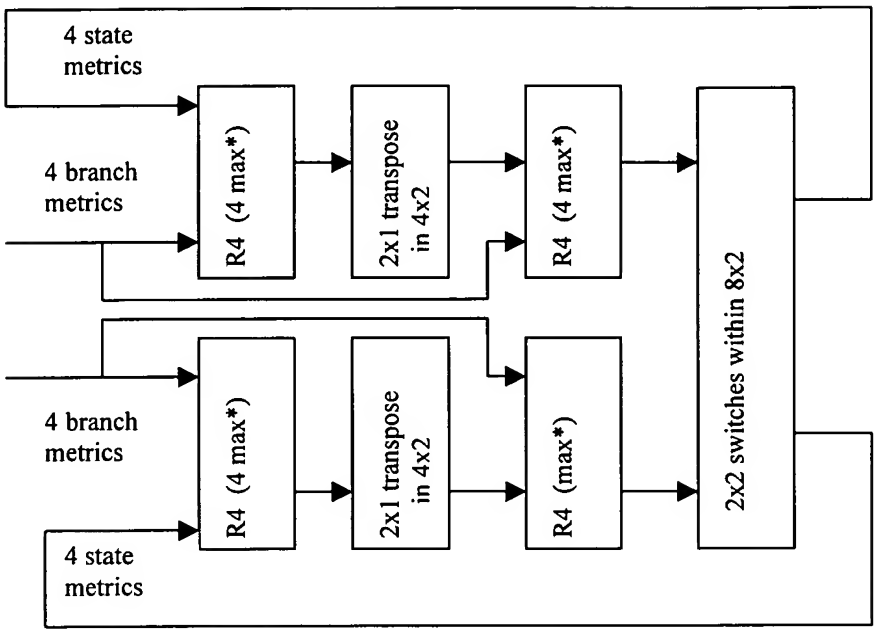

Figure 3b

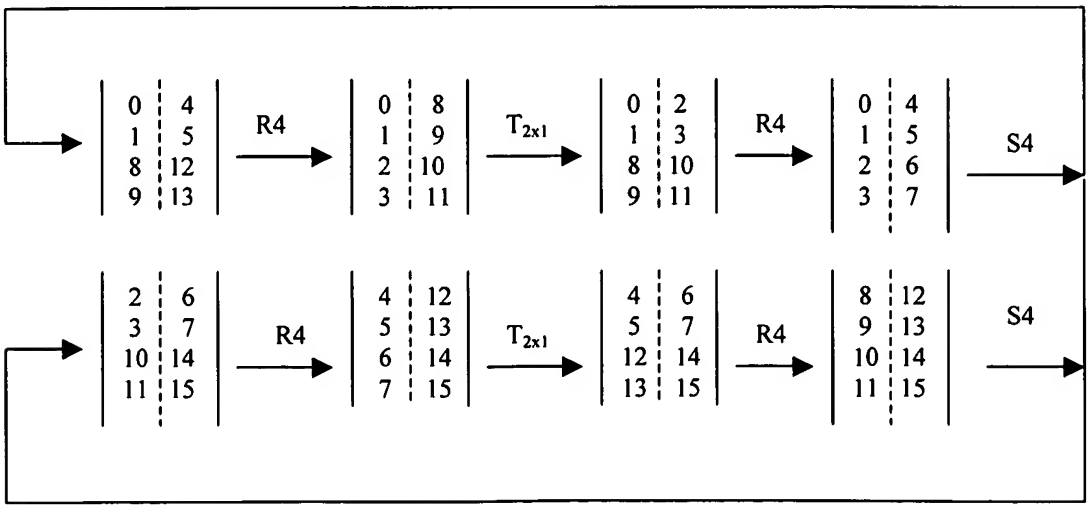

Figure 3c first architecture beta block

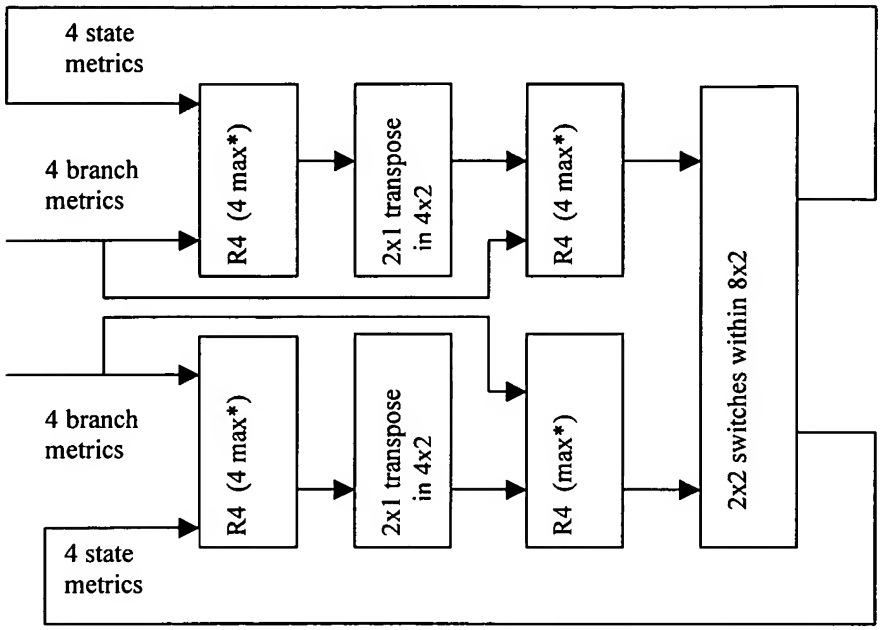

Figure 3d

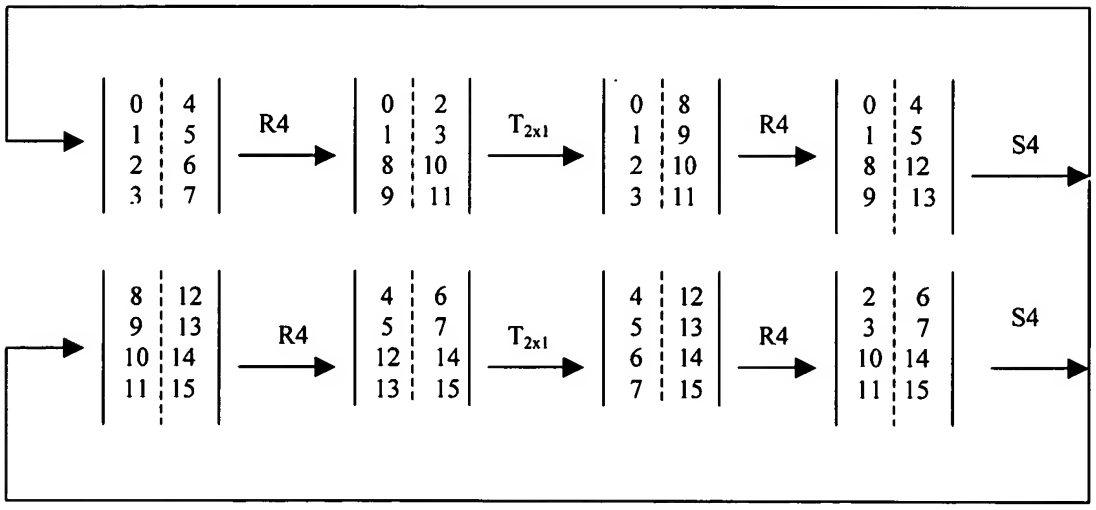

Figure 3e second architecture beta block

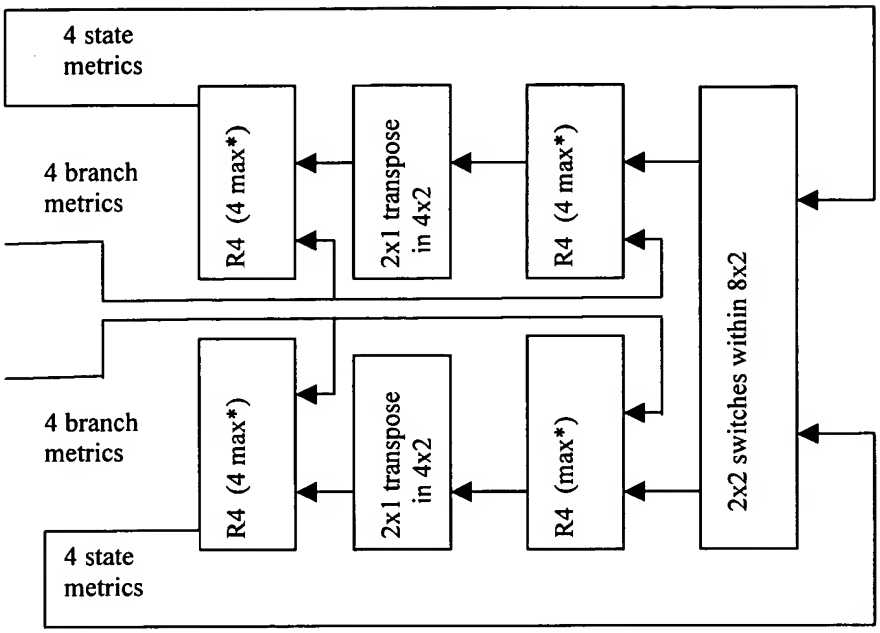

Figure 3f

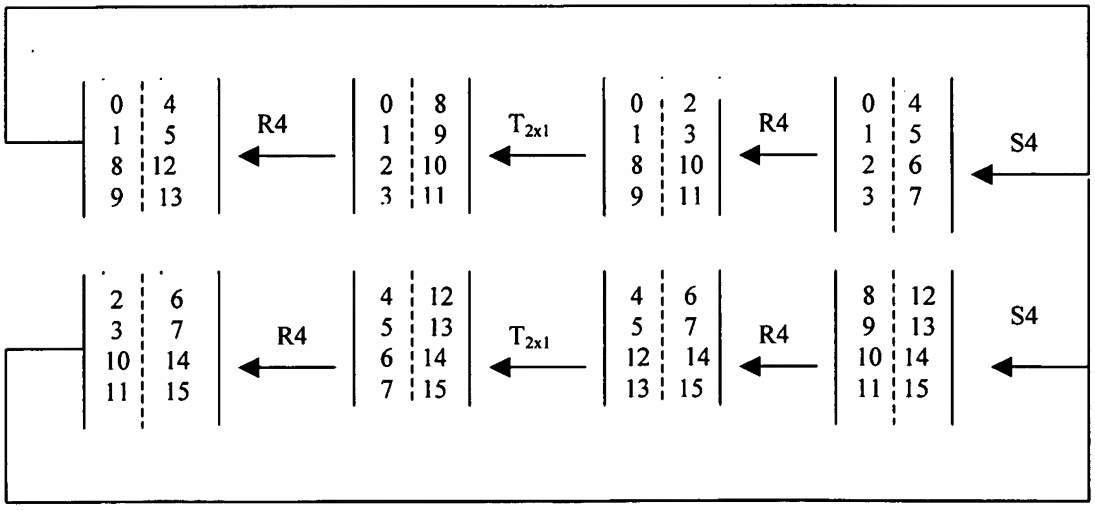

Figure 3g cascade extrinsic subblock

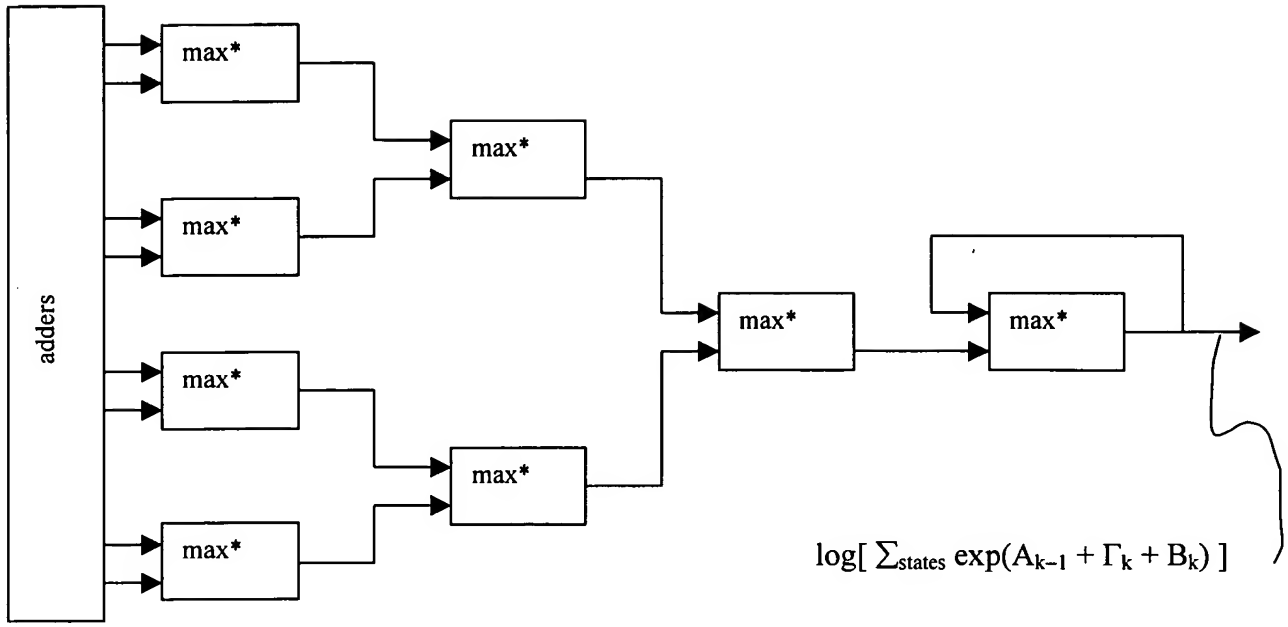

Figure 4 alpha block

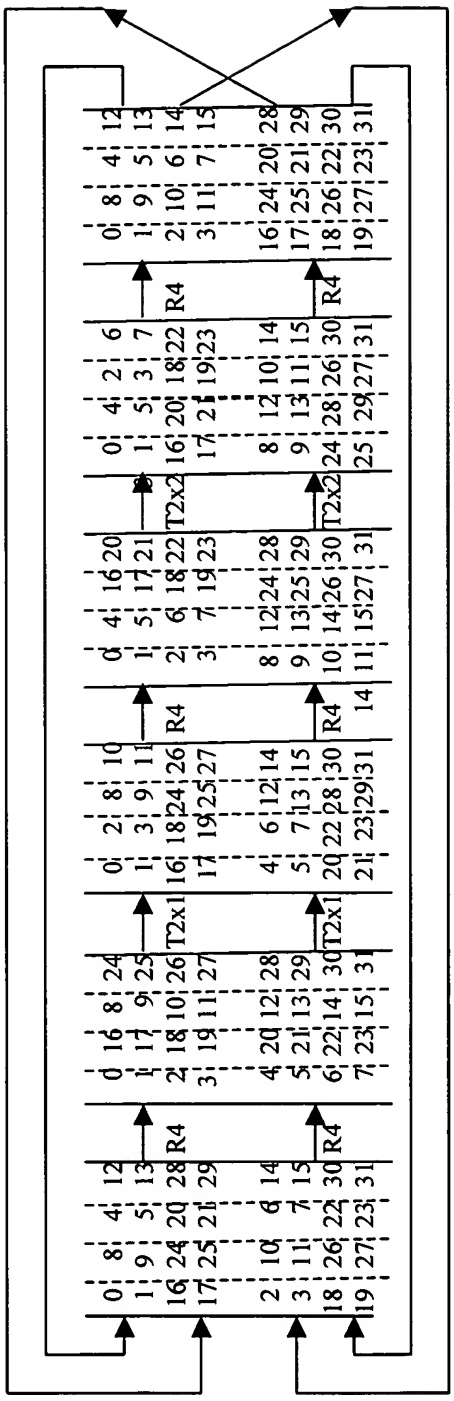

Figure 5a alpha block

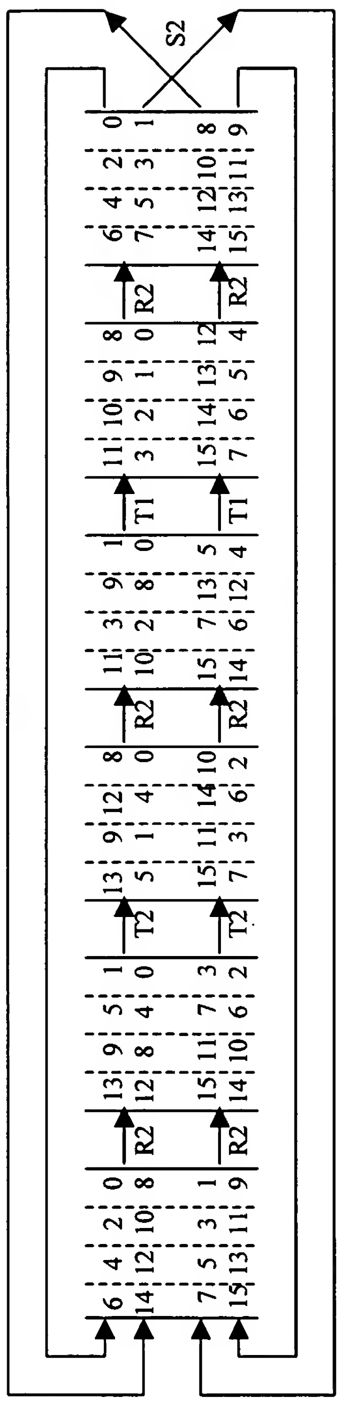

Figure 5b beta block

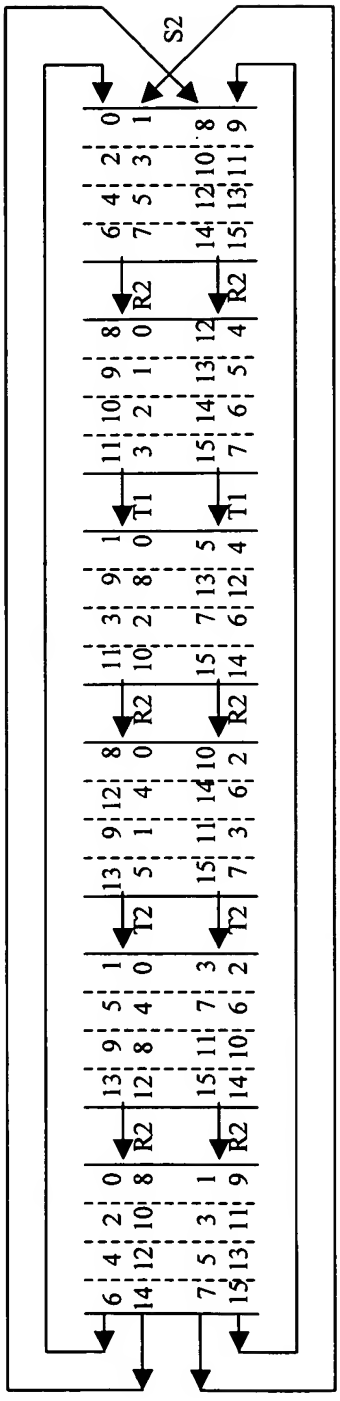

Figure 5c extrinsics block